Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 4 with the following amended paragraph:

The six micro engines 22a-22f access ~~either~~ the SDRAM ~~16a or~~ 16a, SRAM 16b, or Flash ROM 16c based on characteristics of the data. Thus, low latency, low bandwidth data is stored in and fetched from SRAM 16b, whereas higher bandwidth data for which latency is not as important, is stored in and fetched from SDRAM 16a. The micro engines 22a-22f can execute memory reference instructions to either the SDRAM controller 26a or SRAM controller ~~16b~~ 26b.

Please replace the paragraph beginning at page 10, line 27 with the following amended paragraph:

The "immed_data" field represents 10 bits of the immediate data to be written to the control and status register (CSR); valid immed_data values are 0 through 0x3FF. The "csr_addr" field represents the symbolic names ~~that~~ of the corresponding CSRs. The "optional_token" field contains an "indirect_ref" parameter that indicates overriding qualifiers or additional qualifiers, fully described below, are associated with this reference.

Please replace the abstract at page 17 with the following amended abstract:

A method of operating a processor to perform direct write operations to the processor's registers, including, for example the processor's control and status registers. The method includes ~~including~~ receiving data in a processing thread having a processing thread number and ~~shifting~~ loading the data into selected bits of a register ~~corresponding~~ according to the processing thread number.